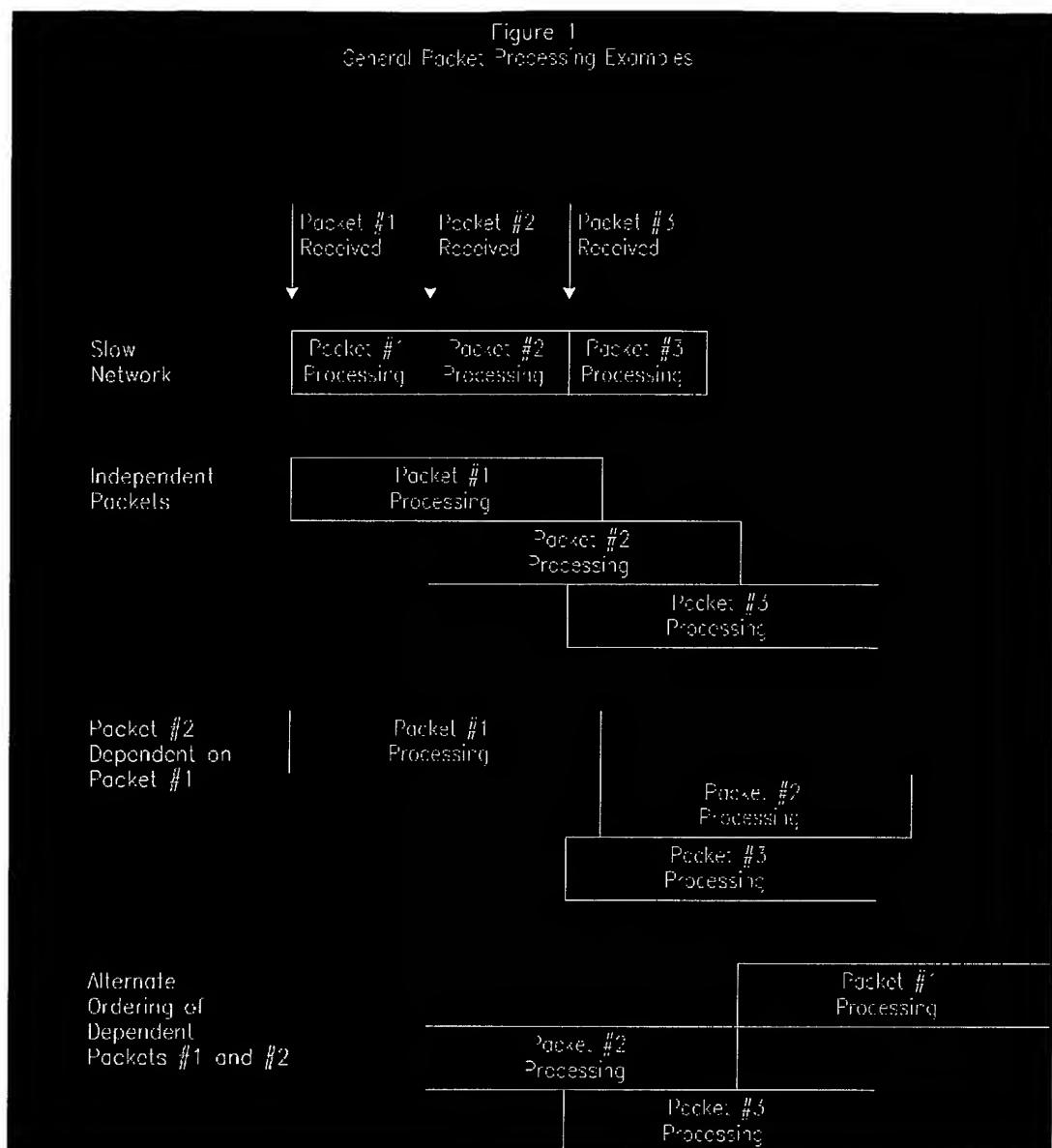


Figure 1  
General Packet Processing Examples



**Figure 2**  
Optimal Overlap of Dependent Packets

No Overlap Possible	Rd A	Packet #1 Processing	Wr A		Rd A	Packet #2 Processing	Wr A	
Non Optimal Overlap		Rd A	Packet #1 Processing	Wr A		Rd A	Packet #2 Processing	Wr A
Optimal Overlap		Rd A	Packet #1 Processing	Wr A		Rd A	Packet #2 Processing	Wr A
Alternate Ordering Optimal Overlap				Rd A	Packet #1 Processing	Wr A		
	Rd A	Packet #2 Processing	Wr A					

Figure 3  
Hardware Enforced Virtual Sequentiality Block Diagram

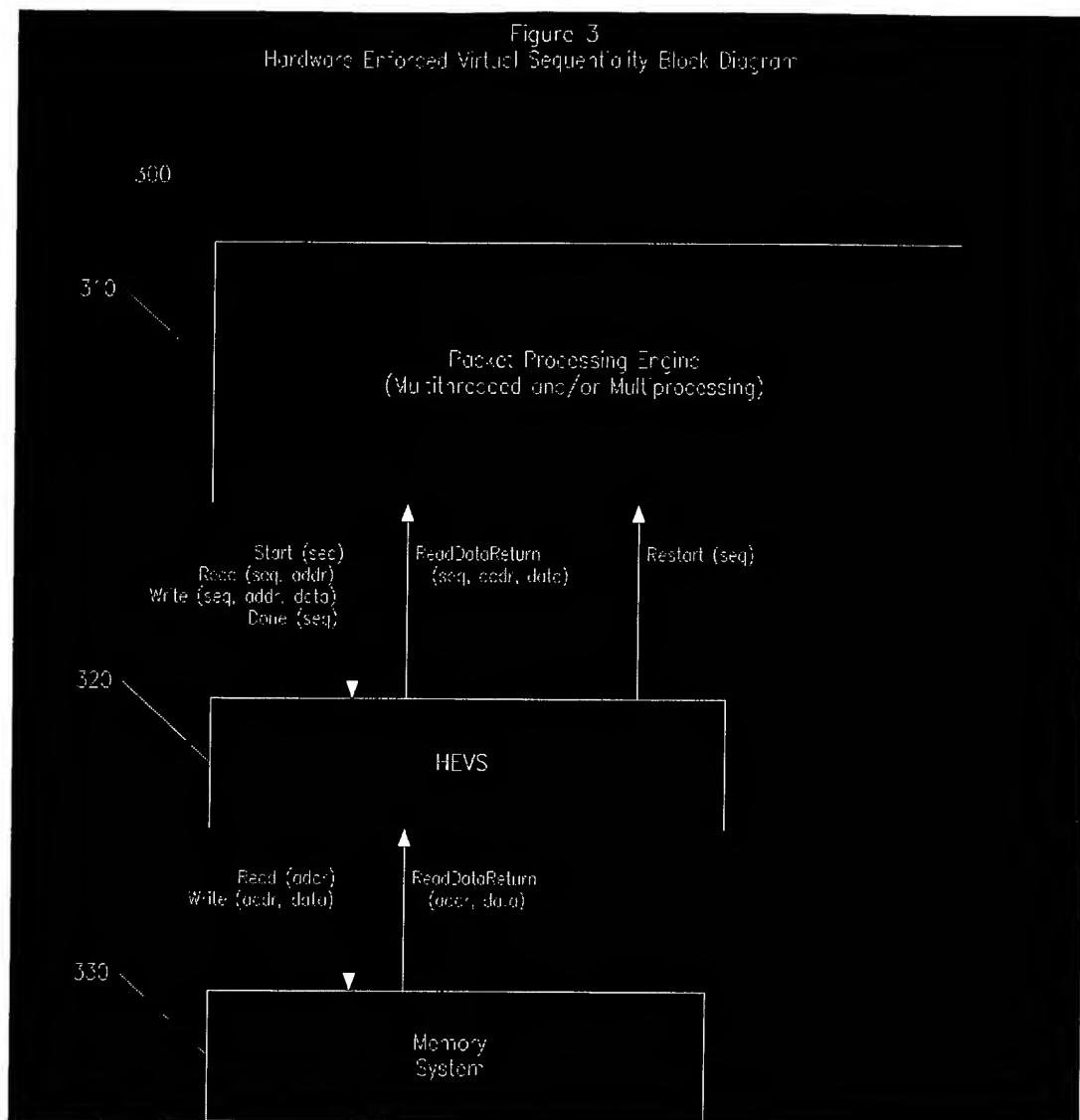


Figure 4  
Hardware Enforced Virtual Sequentiality Mechanism

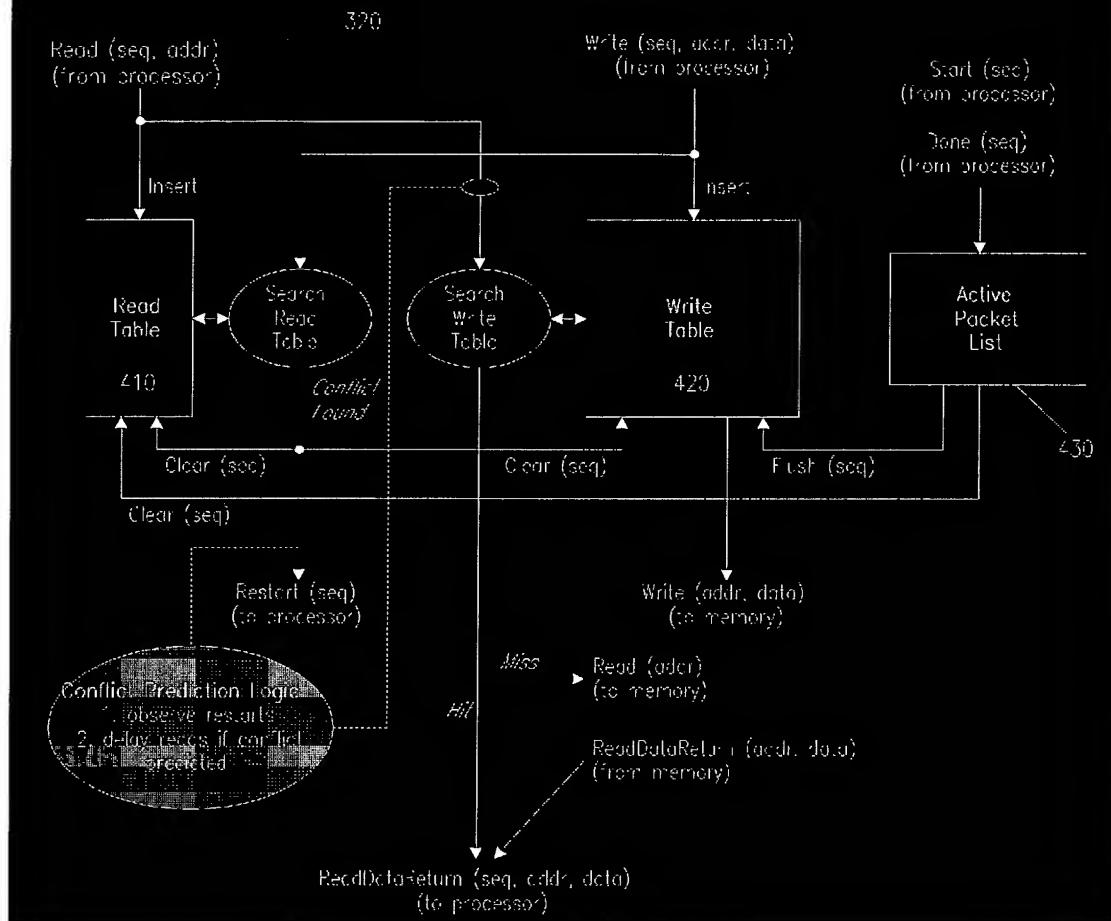


Figure 5  
Read Table and Write Table Detail

**Read Table**

	Seq.	Addr.
p:	1	A
q:	2	B
s:	3	B
t:	2	A

**Write Table**

	Seq	Accr	Done	Depend
r:	2	E	X	3
u:	1	A	X	(s, t)

**Time Sequence:**

1. Packet #1 reads location A  
Entry p: created in Read Table  
Write Table is searched, no matches found so memory read is performed
2. Packet #2 reads location B  
Entry q: created in Read Table  
Write Table is searched, no matches found so memory read is performed
3. Packet #2 writes location B  
Entry r: created in Write Table  
Read Table is searched, no conflicts found
4. Packet #3 reads location B  
Entry s: created in Read Table  
Write Table is searched, entry r: found, done X forwarded and dependency list updated
5. Packet #2 reads location A  
Entry t: created in Read Table  
Write Table is searched, no matches found so memory read is performed
6. Packet #1 writes location A  
Entry u: created in Write Table  
Read Table is searched for newer sequence read, entry r: t: is found  
Conflict is signaled to processor, Packet #2 is restarted  
Entry q: and all other sequence 2 entries are deleted  
Deletion of entry r: triggers Packet #3 restart signaled

Figure 6  
Conflict Detection Processing Examples

